Amendments to the Specification:

Please replace paragraphs 0034, 0055, 0071, 0098, 0101, 0102, 0108, 0109, 0123, 0127, 0131, 0141, 0150, 0155, 0157, 0158, 0159, 0162, 0163, 0164, 0165, 0175, and 0177 with the following amended paragraphs:

[0034] In a first aspect of the present invention, a method for rf power amplifying comprises: series connecting upper and lower solid-state current devices; the series connecting step comprises connecting a lower-voltage terminal of the upper solid-state current device to an rf choke, and connecting the rf choke to a higher-voltage terminal of the lower solid-state current device; separately amplifying rf signals in the solid-state current devices at a selected operating frequency; rf decoupling the solid-state current devices; the rf decoupling step comprises ~~step~~ providing a capacitance between the lower-voltage terminal and an electrical ground; and the rf decoupling step further comprises making an rf effective series resistance of the capacitance lower than that of any porcelain capacitor that resonates at the selected operating frequency.

[0055] FIGURE 19 is a model for simulating a microwave capacitor;

[0071] Referring now to FIGURES 1 and 1A, with regard to the potentiometer VD1 of FIGURE 1A, if any drain-to-source bias imbalances occur between the FETs, Q1 and Q2, when applying an rf signal, the drain-to-source biases of the FETs Q1 and Q2 may be equalized by adjusting a wiper 122 of the potentiometer VD1, thereby adjusting the gate-to-source bias of both FETs, Q1 and Q2.

[0098] Referring now to FIGURE 12, an rf power amplifier 130 includes like-named and like-numbered parts as those in the rf power amplifier 10 of FIGURE 1, except as specified. More particularly, the rf power amplifier 130 includes a three-way power splitter 132, a three-way power combiner 134 that is optional, a solid-state current device, gallium arsenide FET, GaAsFET, or FET, Q5, a decoupling capacitor C10, an rf choke L8, coupling capacitors C11 and C12, ~~and~~ an rf choke L9, and the voltage divider FD2.

[0101] Referring now to FIGURE 13, an rf power amplifier 140 includes like-named and like-numbered components as those shown in FIGURE 6, except that a voltage controlled oscillator, or VCO, 142 replaces the FET Q4, and ~~both~~ a pair of jumper terminals 144 and a pair of jumper terminals 146 are added. The VCO 142 includes a varactor VC1, an inductor L10, a capacitor C13, the rf choke L6, a solid-state current device, gallium arsenide FET, GaAsFET, or FET Q6, and the resistor R5. The VCO 142 produces an rf output signal that is varied in frequency by changing a control voltage V_C applied to the varactor VC1.

[0102] As shown in FIGURE 13, the VCO 142 drives the ~~input terminal~~ rf input RF_{IN} of the power splitter 12. However, if the VCO 142 does not provide sufficient rf power for the power splitter 12, a decoupling capacitor C16 may be added by interconnecting the pair of jumper terminals 144.

[0108] By placing the FETs Q4 and Q6 in parallel, these two FETs share the current flow through the FETs Q1 and Q2, thereby reducing the need to shunt additional current flow past the FETs Q4 and Q6 by the use of a parallel-connected resistor, resistor R13. That is, the combined current flow through the FETs Q4 and Q6, for some applications, may still be lower than the current flow that is desired for the FETs Q1 and Q2, but the need for current shunting will be less for the FIGURE 15 embodiment than it is when the FETs Q4 and Q6 are connected in series, as in FIGURE 14.

[0109] Referring now to FIGURE 16, an rf power amplifier 170 is provided for relatively-low power applications. The rf power amplifier 170 includes like-named and like-numbered components as those shown and described in conjunction with FIGURE 13, except for omission of the FET Q2, the power splitter 12, and the power combiner 14, and except for the addition of an npn bipolar transistor Q7, a pair of jumper terminals 172, and a resistor R16.

[0123] The selection of the decoupling capacitors and chokes are both critical to the rf performance of the circuit, particularly for high power rf amplifiers, although selection of decoupling capacitors is the most critical. Decoupling capacitors, such as the decoupling capacitors ~~C5, D6, C8, C10, C14, and C16~~ C5, C6, C8, C10, C14, and C16 are selected for both resonant

frequencies at or very near to the circuit operating frequency and the lowest possible effective (or equivalent) series resistances (ESRs). The rf chokes, such as the rf chokes L1, L2, L3, and L4, preferably are inductors with self-resonant frequencies at or very near to the circuit operating frequency.

[0127] This self-resonant feature is used in the circuit to prevent the rf signal from coupling onto the dc bias lines and to ~~aide~~ aid the decoupling capacitors in preventing rf crosstalk between the two, or more, FETs. For narrow-band operation, very high-Q inductors are desired to maximize series impedance. Quarter wave transformers may also be used for this function in narrow-band applications. For broad-band operation, lower-Q inductors are desired to obtain a high impedance across a larger bandwidth. In either application, the inductor must be capable of passing the maximum dc current without breakdown.

[0131] The rf impedance of a capacitor at self-resonant frequency is equal to the ESR. As in the case of the inductor, the quality factor Q of a capacitor is the ratio of a capacitor's reactance to its ESR, or alternatively the quality factor Q is 1/DF where DF is the dissipation factor of the capacitor. High-Q capacitors, with very low ESR, have very low self-resonant impedances, but for only a narrow bandwidth. Lower-Q capacitors, with higher ESR, have lower self-resonant impedances for a much broader bandwidth. Presently, the preferred capacitor dielectric to minimize capacitor ESR is porcelain. Porcelain has a dissipation factor, DF, of 0.00007, the lowest of all currently available capacitor dielectrics.

[0141] Model 600S capacitors that are available from *American Technical Ceramics*, their self resonant frequencies, their capacities, and their effective series resistances, are included in the following table.

[0150] Referring now to FIGURE 21, a thermally conductive, electrically insulating pad 190 is inserted between a FET mounting flange 192 of a FET 194 and a heat sink, or chassis, 196 to allow the dissipated heat of the FET 194 to flow from the FET 194 to the heat sink 196 while maintaining electrical isolation. The electrical insulating material of the pad 190 should have no higher than ~~0.5 °C/Watt~~ 0.5° C/Watt thermal resistance. An insulating material with a higher thermal resistance, combined with the thermal resistance

of the FET 194 and the ambient temperature, may result in the internal junction temperature of the FET 194 being excessive, thereby causing reduced reliability or destruction of the FET 194.

[0155] If the phase control voltage is lowered to ~~0 volts~~ 0.0 volts dc by the phase control 206, ~~10 volts~~ 10.0 volts dc will be applied ~~appear~~ across the FET Q1, and ~~0 volts~~ 0.0 volts dc will be applied across the FET Q2. Since the gain of FETs, such as the GaAsFETs, Q1 and Q2, is approximately a linear function of the drain-to-source voltage, an rf output of the FET Q1 will be at maximum gain while an rf output of the FET Q2 will be at minimum.

[0157] If the phase control voltage is now raised to 10.0 volts dc by the phase control 206, 0.0 volts dc will be applied across the FET Q1, and 10.0 volts dc will be applied across the FET Q2. The FET Q1 will now be at a minimum gain while the FET Q2 will be at maximum. In this case the output of the in-phase power combiner 204 will be in phase with a lower terminal 210 of the quadrature power splitter 202. That is, the phase will have been shifted 90 degrees. Again, half of the power is delivered to the rf output RF_{OUT} ~~terminal~~ and half is delivered to the internal or external load.

[0158] If the phase control voltage is set to 5.0 volts dc by the phase control 206, 5.0 volts dc will be applied across both the FET Q1 and the FET Q2, and both FETs will operate at half gain. In this case an upper input terminal 212 and a lower input terminal 214 to the in-phase power combiner 204 will be equal in amplitude but 90 degrees out of phase.

[0159] At this time, the rf output RF_{OUT} ~~RF_{OUT} terminal~~ of the in-phase combiner 204 remains at half power but is 45 degrees out of phase with the upper input terminal 212. As before, half of the power will be delivered to the internal or external load.

[0162] Referring now to FIGURE 23, a variable phase-shifting rf amplifier 220 has a wider phase range than the variable phase-shifting rf amplifier 200 of FIGURE 22. The variable phase-shifting rf amplifier 220 includes a 180 degree power splitter 222, 90 degree power splitters 224A and 224B, solid-state current devices, or GaAsFETs, Q1, Q2, Q5, and Q8, 0 degree power combiners 228A and 228B, and a 0 degree power combiner 230. In addition, the variable phase-shifting rf amplifier 220 includes coupling

capacitors, decoupling capacitors, and rf chokes as shown in ~~FIGURE 23~~ FIGURE 22, and as taught in conjunction with various ones of the preceding embodiments.

[0163] If phase-shifting voltages V_{PS1}, V_{PS2}, and V_{PS3} are all set to 0.0 volts dc, 10.0 volts dc will appear across the FET Q1 and 0.0 volts dc will appear across the FETs Q2, Q5, and Q8. Since the gain of the FETs, Q1, Q2, Q5, and Q8 is approximately a linear function of the applied voltage from drain to source, the FET Q1 will be at maximum gain while the ~~FETs Q2,Q5, and Q8~~ FETS Q2, Q5, and Q8 will be at minimum. The rf output RF_{OUT} ~~terminal~~ will then be at 0 degrees (disregarding the inversion of the FET Q1) relative to the rf input RF_{IN}.

[0164] If the phase-shifting voltage V_{PS1} is now raised to 10.0 volts dc and the phase-shifting voltages V_{PS2} and V_{PS3} remain at ~~0 volts~~ 0.0 volts dc, 10.0 volts dc will appear across the FET Q2, and 0.0 volts dc will appear across the ~~FETs Q1,Q5, and Q8~~ FETS Q1, Q5, and Q8. The FET Q2 will now be at maximum gain while the ~~FETs Q1,Q5, and Q8~~ FETS Q1, Q5, and Q8 will be at minimum. In this case the rf output RF_{OUT} will be at 90 degrees relative to the rf input RF_{IN} (again disregarding the inversion of the FET Q2).

[0165] Similarly to FIGURE 22, if the phase-shifting voltage V_{PS1} is at 5.0 volts dc, and the phase-shifting voltages V_{PS2} and V_{PS3} are at 0.0 volts dc, the rf output RF_{OUT} will be at 45 degrees relative to the rf input RF_{IN}. By proper application of the ~~phase control~~ phase-shifting voltages V_{PS1}, V_{PS2}, and V_{PS3}, the phase of the variable phase-shifting rf amplifier ~~200~~ 220 can be made to vary monotonically and reasonably linearly from 0 degrees to 270 degrees.

[0175] More succinctly, the present invention can be characterized as connecting a plurality of field-effect devices in series for dc operation while the same devices operate in parallel for rf operation. Additionally, the present invention provides a method for minimizing the rf impedance from a field-effect device source to a circuit ground, thereby maximizing dc-rf conversion efficiency while minimizing interference between field-effect devices, and between field-effect devices and power supply, by design and selection of decoupling capacitors and rf chokes.

[0177] U.S. Patent ~~Application Serial 10/028,844, filed December 20, 2001~~ No. US 6,683,499 B2, which issued January 27, 2004, is incorporated herein by reference thereto.